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EXAMINER	
QUINTO, KEVIN V	

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2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,294	TU ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) *31-44* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-11,14-18 and 21-44* is/are rejected.

7)☒ Claim(s) *7,12,13,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20 October 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 31-44 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on March 17, 2006.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 8 and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 8 recites the limitation "wherein the at least one MIM capacitor comprises an array of memory devices" but this limitation appears to be inaccurate since a capacitor in itself cannot form an array of memory devices. The examiner has interpreted this limitation to mean that *the at least one MIM capacitor is part of an array of memory devices.*

5. Claim 30 recites the limitation "the at least one third insulating layer" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

6. The examiner is unable to determine the metes and bounds of this claim since "the at least one third insulating layer" is not previously described in claims 27 or 29.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 2, 3, 8, 9, 10, 15, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Maeda et al. (United States Patent Application Publication No. US 2002/0017673 A1).

9. In reference to claim 1, Maeda et al. (United) discloses a device which meets the claim. Figure 1 of Maeda illustrates a semiconductor device with a first insulating layer (17) formed over a workpiece (1). There is at least one second insulating layer (18) formed over the first insulating layer (17). At least one metal-insulator-metal (MIM) capacitor is formed in the first insulating layer (17) and the at least one second insulating layer (18). The at least one MIM capacitor has a first conductive layer (20), a dielectric layer (21) disposed over the first conductive layer (20), and a second conductive layer (22) formed over the dielectric layer (21). The first conductive layer (20) extends completely to a top surface of the at least one second insulating layer (18).

10. With regard to claim 2, the first conductive layer (20) and the second conductive layer (22) comprise refractory metals and nitrides of these metals which meet the claim (p. 7, paragraph 72).

11. With regard to claim 3, the dielectric layer (21) is formed of several materials which meet the claim (p. 7, paragraph 72).

12. So far as understood in claim 8, the at least one MIM capacitor is part of an array of memory devices with the array having a dimension greater than 2×1 (p. 5, paragraph 59).

13. In reference to claim 9, the first conductive layer (20) comprises a bottom electrode, the dielectric layer (21) comprises a capacitor dielectric, and the second conductive layer (22) comprises a top electrode. Maeda discloses the use of a chemical-mechanical polish (CMP) process to form the bottom electrode (p 7, paragraph 71).

14. With regard to claim 10, Maeda discloses that the device is a dynamic random access memory device (DRAM).

15. In reference to claims 15 and 17, figure 1 of Maeda clearly shows that the workpiece comprises a plurality of elements (transistors) formed therein. A third insulating layer (13) is formed between the workpiece and the first insulating layer (17), further comprising at least one first conductive region (16) disposed in the third insulating layer (13) abutting the first conductive layer (20) of the at least one MIM capacitor, wherein the at least one first conductive region (16) and the first conductive layer (20) comprise a bottom plate of the at least one MIM capacitor. The first

conductive region (16) couples the at least one MIM capacitor to an element on the workpiece.

16. Claims 1-6, 9, 10, 11, 14-18, and 22-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Jin et al. (United States Patent Application Publication No. US 2003/0183862 A1).

17. In reference to claim 1, Jin et al. (United States Patent Application Publication No. US 2003/0183862 A1, hereinafter referred to as the "Jin" reference) discloses a device which meets the claim. Figures 10H and 11B of Jin each illustrates a semiconductor device with a first insulating layer (218) formed over a workpiece (not shown). There is at least one second insulating layer (220 or 224 or 230 or 232 or 234) formed over the first insulating layer (218). At least one metal-insulator-metal (MIM) capacitor is formed in the first insulating layer (218) and the at least one second insulating layer (220 or 224 or 230 or 232 or 234). The at least one MIM capacitor has a first conductive layer (238), a dielectric layer (240) disposed over the first conductive layer (238), and a second conductive layer (242) formed over the dielectric layer (240). The first conductive layer (238) extends completely to a top surface of the at least one second insulating layer (220 or 224 or 230 or 232 or 234).

18. With regard to claim 2, the first conductive layer (238) and the second conductive layer (242) comprise refractory metals and nitrides of these metals which meet the claim (p. 8, paragraph 136).

19. With regard to claim 3, the dielectric layer (240) is formed of several materials which meet the claim (p. 8, paragraph 137).

20. In reference to claim 4, the at least one second insulating layer (220 or 224 or 230 or 232 or 234) comprises five or more insulating layers in which the MIM capacitor is formed in its entirety.

21. With regard to claim 5, the workpiece comprises a plurality of elements formed therein (p. 7, paragraph 125). A third insulating layer (210) is formed between the workpiece and the first insulating layer (218). There is at least one first conductive region (212, 214a) disposed in the third insulating layer (210) abutting the first conductive layer (238) of the at least one MIM capacitor, wherein the at least one first conductive region (212, 214a) and the first conductive layer (238) comprise a bottom plate of the at least one MIM capacitor. Furthermore it is understood that the first conductive region (212, 214a) couples the at least one MIM capacitor to an element on the workpiece.

22. In reference to claim 6, the third insulating layer (210) comprises a first metallization layer of the semiconductor device (p. 7, paragraph 125). The first insulating layer (218) comprises a first via layer of the semiconductor device, wherein the second insulating layer (220 or 224 or 230 or 232 or 234) comprises a second metallization layer of the semiconductor device. The at least one MIM capacitor is formed in the first via layer (218) and the second insulating layer (220 or 224 or 230 or 232 or 234) of the semiconductor device.

23. In reference to claim 9, the first conductive layer (238) comprises a bottom electrode, the dielectric layer (240) comprises a capacitor dielectric, and the second conductive layer (242) comprises a top electrode. The examiner notes the limitation

with regard to the use of a chemical-mechanical polish (CMP) process to form the top and bottom electrodes. However this places claim 9 into the form of a **product-by-process claim**:

> Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Thorpe*, 227 USPQ 964, 966; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi* et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 2113.

Claim 9 does not distinguish over the Jin reference regardless of the process used to form the top and bottom electrodes, because only the final product is relevant, and not the process of making such as a chemical-mechanical polishing (CMP).

24. With regard to claim 10, Jin discloses that the capacitor is intended for use in a mixed-mode device (p. 1, paragraph 2).

25. In reference to claim 11, the workpiece comprises a first region and a second region, wherein the at least one MIM capacitor is formed over the first region, further comprising conductive regions (228 – both figures 10H and 11B, and although not shown to completion; the opening (250) in figure 10B) formed in the first insulating layer (218) and the second insulating layer (220 or 224 or 230 or 232 or 234) over the second region of the workpiece.

26. With regard to claim 14, the second insulating layer (220 or 224 or 230 or 232 or 234) comprises a recessed region between at least two adjacent MIM capacitors, the at least two MIM capacitors having top plates comprised of the second conductive layer (242), wherein the second conductive layer fills the recessed region of the second

insulating layer, electrically coupling together the top plates of at the least two adjacent MIM capacitors.

27. In reference to claims 15 and 17, the workpiece comprises a plurality of elements formed therein (p. 7, paragraph 125). A third insulating layer (210) is formed between the workpiece and the first insulating layer (218), further comprising at least one first conductive region (212, 214a) disposed in the third insulating layer (210) abutting the first conductive layer (238) of the at least one MIM capacitor, wherein the at least one first conductive region (212, 214a) and the first conductive layer (238) comprise a bottom plate of the at least one MIM capacitor. Furthermore it is understood that the first conductive region (212, 214a) couples the at least one MIM capacitor to an element on the workpiece.

28. With regard to claim 16, the at least one first conductive region (212, 214a) comprises a conductive barrier layer (212) and a conductive material (214a) disposed over the conductive barrier layer (212).

29. In reference to claim 18, the first conductive region (212, 214a) and the third insulating layer (210) comprise a first metallization layer of the semiconductor device (p. 7, paragraph 125). The first insulating layer (218) comprises a first via layer of the semiconductor device, wherein the second insulating layer (220 or 224 or 230 or 232 or 234) comprises a second metallization layer of the semiconductor device. The at least one MIM capacitor is formed in the first via layer (218) and the second metallization layer (220 or 224 or 230 or 232 or 234) of the semiconductor device.

30. In reference to claim 22, Jin (United States Patent Application Publication No. US 2003/0183862 A1) discloses a device which meets the claim. Figures 10H and 11B of Jin each illustrates a semiconductor device with a first insulating layer (218) formed over a workpiece (not shown). There is at least one second insulating layer (224) formed over the first insulating layer (218). There is at least one third insulating layer (232) formed over the second insulating layer (224). At least one metal-insulator-metal (MIM) capacitor is formed in the first insulating layer (218), the second insulating layer (224), and the third insulating layer (232). The at least one MIM capacitor has a first conductive layer (238), a dielectric layer (240) disposed over the first conductive layer (238), and a second conductive layer (224) formed over the dielectric layer (240).

31. In reference to claim 23, the first insulating layer (218) comprises a first via layer of the semiconductor device, wherein the second insulating layer (224) comprises a first metallization layer of the semiconductor device. The third insulating layer (232 in figure 10H) comprises at least one second via layer and at least one second metallization layer of the semiconductor device. The at least one MIM capacitor extends through the entire thicknesses of the first via layer (218), the first metallization layer, the at least one second via layer, and the at least one second metallization layer.

32. With regard to claim 24, the workpiece comprises a plurality of elements formed therein (p. 7, paragraph 125). A fourth insulating layer (210) is formed between the workpiece and the first insulating layer (218). There is at least one first conductive region (212, 214a) disposed in the fourth insulating layer (210) between the first conductive layer (238) of the at least one MIM capacitor and an element in the

workpiece. Furthermore it is understood that the first conductive region (212, 214a) couples the at least one MIM capacitor to an element on the workpiece. The at least one first conductive region (212, 214a) and the first conductive layer (238) comprise a bottom plate of the at least one MIM capacitor.

33. In reference to claim 25, the fourth insulating layer (210) comprises a first metallization layer of the semiconductor device (p. 7, paragraph 125). The first insulating layer (218) comprises a first via layer of the semiconductor device, wherein the second insulating layer (224) comprises a second metallization layer of the semiconductor device. The at least one third insulating layer (232 – see figure 10H) comprises at least one second via layer and at least one third metallization layer. The at least one MIM capacitor extends through the entire thicknesses of the first via layer (218), the first metallization layer, the at least one second via layer, and the at least one second metallization layer.

34. With regard to claim 26, the top of the third insulating layer (232) comprises a recessed region between at least two adjacent MIM capacitors, the at least two MIM capacitors having top plates comprised of the second conductive layer (242), wherein the second conductive layer fills the recessed region of top of the third insulating layer (232), electrically coupling together the top plates of at the least two adjacent MIM capacitors.

35. In reference to claim 27, Jin (United States Patent Application Publication No. US 2003/0183862 A1) discloses a device which meets the claim. Figures 10H and 11B of Jin each illustrates a semiconductor device with a first insulating layer (218, 224) formed

over a workpiece (not shown). There is a plurality of metal-insulator-metal (MIM) capacitors is formed in the at least one first insulating layer (218). The plurality of MIM capacitors has a first conductive layer (238), a dielectric layer (240) disposed over the first conductive layer (238), and a second conductive layer (242) formed over the dielectric layer (240). The second conductive layer (242) comprises a top plate of the plurality of MIM capacitors. A top of the least one first insulating layer (218, 224) comprises a recessed region between at least two adjacent MIM capacitors. The second conductive layer fills the recessed region of top of the first insulating layer (218, 224), electrically coupling together the top plates of at the least two adjacent MIM capacitors.

36. With regard to claim 28, the at least first insulating layer (218, 224) comprises at least two insulating layers. One first insulating layer (218) comprises a via layer of the semiconductor device while the other first insulating layer (224) comprises an interconnect layer formed over the via layer.

37. In reference to claim 29, the workpiece comprises a plurality of elements formed therein (p. 7, paragraph 125). At least one second insulating layer (210) is formed between the workpiece and the first insulating layer (218, 224). A conductive region (212, 214a) is formed in each of the least one second insulating layer (210) and is electrically coupled to the first conductive layer (238) of the at least one MIM capacitor. The conductive region (212, 214a) and the first conductive layer (238) comprise a bottom plate of the at least one MIM capacitor. Furthermore it is understood that the

conductive region (212, 214a) couples the at least one MIM capacitor to an element on the workpiece.

Claim Rejections - 35 USC § 103

38. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

39. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda et al. (United States Patent Application Publication No. US 2002/0017673 A1) in view of Stumborg et al. (USPN 6,077,775).

40. With regard to claim 16, Maeda discloses the use of a tungsten conductive region (p. 5, paragraphs 53-54) but not a conductive region which is made with a conductive barrier layer and a conductive material disposed over the conductive barrier layer. However the use of such contact structure is well known the art. Stumborg et al. (USPN 6,077,775, hereinafter referred to as "Stumborg" reference) discloses a conductive region formed of a conductive material (45), copper, which is disposed over a conductive barrier layer (49) in figure 8. Stumborg discloses that copper has the advantage of a greater conductivity than aluminum or tungsten which allows smaller sized conductors that are needed since the density of components in integrated circuits is increasing (column 1, lines 58-65). In view of Stumborg, it would therefore be

obvious to implement a conductive region which is formed of a conductive material that is disposed over a conductive barrier layer in the device of Maeda.

41. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda et al. (United States Patent Application Publication No. US 2002/0017673 A1) in view of Yang et al. (USPN 6,417,537 B1).

42. With regard to claim 21, Maeda discloses the use of a conductive material for the second conductive layer or top electrode of the MIM capacitor but does not disclose the use of a conductive layer comprising a conductive barrier layer and a conductive material disposed over the conductive barrier layer. However the use of such an electrode structure is well known the art. Yang et al. (USPN 6,417,537 B1, hereinafter referred to as "Yang" reference) discloses a top electrode capacitor structure formed of a conductive material (265) which is disposed over a conductive barrier layer (260) in figure 2I. Yang discloses that such an electrode structure protects the top electrode from oxidation (column 10, lines 42-67) which is a known problem in the art (column 2, lines 12-20). In view of Yang, it would therefore be obvious to implement a top electrode for capacitor which is formed of a conductive material that is disposed over a conductive barrier layer in the device of Maeda.

43. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al. (United States Patent Application Publication No. US 2003/0183862 A1) in view of Yang et al. (USPN 6,417,537 B1).

44. With regard to claim 21, Jin discloses the use of a conductive material for the second conductive layer or top electrode of the MIM capacitor but does not disclose the

use of a conductive layer comprising a conductive barrier layer and a conductive material disposed over the conductive barrier layer. However the use of such an electrode structure is well known the art. Yang (USPN 6,417,537 B1) discloses a top electrode capacitor structure formed of a conductive material (265) which is disposed over a conductive barrier layer (260) in figure 2I. Yang discloses that such an electrode structure protects the top electrode from oxidation (column 10, lines 42-67) which is a known problem in the art (column 2, lines 12-20). In view of Yang, it would therefore be obvious to implement a top electrode for capacitor which is formed of a conductive material that is disposed over a conductive barrier layer in the device of Jin.

Allowable Subject Matter

45. Claims 7, 12, 13, 19, and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

46. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious a semiconductor device with a metal-insulator-metal capacitor having the explicit bottom plate electrode and interlevel dielectric layer structures as suggested by the applicant.

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ